IN THE CLAIMS

Please cancel claim 41.

Please add claim 42.

Please amend claims 16, 21-23, 28-35, and 37-39 as follows:

1-15. (Cancelled)

16. (Currently Amended) A process for producing a leadframe configured to be fitted with a semiconductor chip and to be encapsulated with a plastic compound, the process comprising:

providing a leadframe base body;

applying an interlayer attackable by an etchant that comprises one or more individual layers, to the leadframe; and

etching into the surface of the interlayer using the etchant to form a matrix of islands of remaining material of substantially uniform height with voids extending between these islands.

17. (Previously Presented) The process as claimed in claim 16, comprising depositing silver, a silver alloy and/or a silver compound and/or nickel for the interlayer by means of chemical or electrodeposition processes.

18. (Previously Presented) The process as claimed in claim 16, comprising applying silver, a silver alloy and/or a silver compound and/or nickel as a coarse deposit for the interlayer.

19. (Previously Presented) The process as claimed in claim 16, comprising applying the interlayer in the form of one or more individual layers each having a uniform composition.

20. (Previously Presented) The process as claimed in claim 16, comprising wherein the etching is effected as grain boundary etching at the surface of the interlayer and/or is carried out

by selectively etching out at least one of the alloying constituents or the compound components of the silver at the surface of the interlayer.

21. (Currently Amended) The process as claimed in claim 16, comprising wherein the application of the interlayer and the etching are both carried out over the entire surface of the leadframe base body.

22. (Currently Amended) The process as claimed in claim 16, comprising wherein both the application of the interlayer and the etching are carried out selectively at defined locations of the surface of the leadframe base body.

23. (Currently Amended) A process for producing a semiconductor device, comprising:

producing a leadframe base body including, providing the leadframe, applying an interlayer attackable by an etchant that comprises one or more individual layers, to the leadframe base body, and etching into the surface of the interlayer using the etchant to form a matrix of islands of remaining material of substantially uniform height with voids extending between these islands;

placing a semiconductor chip onto the leadframe base body; and

applying a plastic compound as encapsulating housing to the leadframe base body and semiconductor chip.

24. (Previously Presented) The process as claimed in claim 23, comprising depositing silver, a silver alloy and/or a silver compound and/or nickel for the interlayer by means of chemical or electrodeposition processes.

25. (Previously Presented) The process as claimed in claim 23, comprising applying silver, a silver alloy and/or a silver compound and/or nickel as a coarse deposit for the interlayer.

26. (Previously Presented) The process as claimed in claim 23, comprising applying the interlayer in the form of one or more individual layers each having a uniform composition.

27. (Previously Presented) The process as claimed in claim 26, comprising wherein the etching is effected as grain boundary etching at the surface of the interlayer and/or is carried out by selectively etching out at least one of the alloying constituents or the compound components of the silver at the surface of the interlayer.

28. (Currently Amended) The process as claimed in claim 27, comprising wherein the application of the interlayer and the etching are both carried out over the entire surface of the leadframe base body; and

wherein both the application of the interlayer and the etching are carried out selectively at defined locations of the surface of the leadframe base body.

29. (Currently Amended) A ~~leadframe configured to fit with~~ semiconductor device including a semiconductor chip and to be encapsulated with a plastic compound, the ~~leadframe~~ semiconductor device comprising:

a metallic single-piece base body of a leadframe,

at least one interlayer which has been applied to the base body and may comprise one or more individual layers, and

the interlayer having a surface comprising a matrix of islands of remaining material of substantially uniform height with voids extending between these islands.

30. (Currently Amended) The ~~leadframe~~ semiconductor device as claimed in claim 29, wherein in that the interlayer comprises silver, a silver alloy and/or a silver compound and/or nickel.

31. (Currently Amended) The semiconductor device ~~leadframe~~ as claimed in claim 29, comprising wherein the surface of the interlayer ~~typically~~ has a roughness average Ra of between approx. 0.1 µm and approx. 0.9 µm~~, preferably between approx. 0.1 µm and approx. 0.5 µm~~.

32. (Currently Amended) The semiconductor device ~~leadframe~~ as claimed in ~~one of~~ claim 29, comprising wherein the remaining islands at the surface of the interlayer typically have a mean diameter of approx. 0.5 µm.

33. (Currently Amended) The semiconductor device ~~leadframe~~ as claimed in ~~one of~~ claim 29, comprising wherein the voids at the surface of the interlayer typically have a mean width of approx. 2 µm.

34. (Currently Amended) The semiconductor device ~~leadframe~~ as claimed in ~~one of~~ claim 29, comprising wherein the surface of the interlayer typically has a ratio of the surface areas of islands to voids in the range from approx. 2:1 to approx. 1:2.

35. (Currently Amended) A semiconductor device comprising:

a semiconductor chip and having an encapsulation of plastic compound;

~~a leadframe which is configured to be fitted with the semiconductor chip and to be encapsulated with the plastic compound, the leadframe comprising~~ a metallic single-piece base body of a leadframe, and at least one interlayer which has been applied to the base body and may comprise one or more individual layers, and

the interlayer having a surface comprising a matrix of islands of remaining material of substantially uniform height with voids extending between these islands.

36. (Previously Presented) The semiconductor device as claimed in claim 35, comprising wherein the interlayer comprises silver, a silver alloy and/or a silver compound and/or nickel.

37. (Currently Amended) The semiconductor device as claimed in claim 35, comprising wherein the surface of the interlayer ~~typically~~ has a roughness average Ra of between approx. 0.1 μm and approx. 0.9 μm~~, preferably between approx. 0.1 μm and approx. 0.5 μm~~.

38. (Currently Amended) The semiconductor device as claimed in ~~one of~~ claim 37, ~~ecomprising~~ comprising wherein the remaining islands at the surface of the interlayer typically have a mean diameter of approx. 0.5 μm.

39. (Currently Amended) The semiconductor device as claimed in ~~one of~~ claim 38, comprising wherein the voids at the surface of the interlayer typically have a mean width of approx. 2 μm.

40. (Previously Presented) The semiconductor device as claimed in claim 39, comprising wherein the surface of the interlayer typically has a ratio of the surface areas of islands to voids in the range from approx. 2:1 to approx. 1:2.

41. (Canceled)

42. (New) The process as claimed in claim 16, wherein etching into the surface of the interlayer using the etchant includes etching such that the surface of the interlayer has a roughness average Ra of between approximately 0.1 μm and 0.9 μm.